AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Paragraph at page 1, lines 6-12

This application shared a common disclosure with a commonly-owed U. S. Utility Patent Application No. 09/560,364 entitled "A SOURCE SYNCHRONOUS LINK WITH DATA AND CLOCK SIGNALS HAVING THE SAME ELECTRICAL CHARACTERISTICS" naming as inventors Karen Lo, Jeffery A. Benis and Allan R. Desroches, filed concurrently herewith ~~under Attorney Docket No. 10002534-1,~~ the specification of which is herein incorporated by reference.

Paragaph at page 5, lines 7-15

In a ~~stiff~~ still further aspect of the invention a debug system for determining whether source synchronous receiver has properly captured data transmitted from a transmitter is disclosed. The debug system includes a source synchronous transmitter, a source synchronous receiver; and a debut system. The debug system is configured to control said transmitter to transmit data and a data strobe at a first frequency and to transmit a debug bit pattern while holding said differential data strobe at a predetermined logic level. In addition, the debug system includes a data capture storage and analysis device configured to scan said receiver to retrieve and store captured data for comparison with said debug bit pattern.

Paragaph at page 9, lines 11-17

Figure 1A is a block diagram of two processing cores communicating over a source synchronous link 100 in accordance with aspects of the present invention. A first processing node or core 102 includes a source synchronous transmitter 108 and a second processing node or core 104 includes a source synchronous receiver 100. Source synchronous transmitter 108 and source synchronous receiver 110 are connected via a communication channel or link 106. Data is transferred across link 106 along with an accompanying clock. This arrangement is generally referred to ~~generally~~ as a source synchronous link ~~106~~ 100.

Paragaph at page 9, lines 23 to page 10, line 2

Source synchronous transmitter 108 generally includes data transmit logic 112 and differential data strobe transmit logic 114. Data transmit logic 112 manages the transmission of data signals 120 over a data line of ~~source synchronous~~ communication link 106. Differential data strobe transmit logic 114 generates a differential clock or data strobe signal 122 over two clock lines of source synchronous link 106. Source synchronous transmitter 108 receives a local or core clock 116 and, in certain aspects of the invention, a second local or core clock 118. As will be described in detail below, the second clock may be generated internally by transmitter 108 and need not be implemented in all aspects of the present invention.

A4

Paragaph at page 12, lines 20 to 27

Figure 2A is a functional block diagram of differential data strobe transmit logic 114. Differential data strobe transmit logic 114 generates the differential data strobe 122 comprising data strobe signal DS_OUT 210 and inverse data strobe signal DSN_OUT 212 over communication link 106. Differential data strobe transmit logic 114 includes differential data strobe signal generator logic 204 that determines the shape of the waveform of DS_OUT 210 and DSN_OUT 212. Transmit logic 114 also includes strobe stopping logic 202 that controls the signal level states used by signal generator logic 204 ~~205~~ to cause DS_OUT 210 and DSN_OUT 212 to remain halted in a desired logical state.

A5

Paragaph at page 13, lines 19 to 24

As noted, strobe stopping logic 202 provides to differential data strobe signal generator 204 the logic level signals ~~222-228~~ 222, 224, 226, 228 for data strobe signal DS_OUT 210. In this illustrative embodiment, there are a number of command signals generated by processing core 102 that specify when the differential data strobe is to be halted and, preferably, the state in which the differential data strobe signals DS_OUT 210 and DSN_OUT 212 are to be halted.

A6

Paragaph at page 13, line 25 to page 14, line 2

In this embodiment, the data strobe control command signals 160 include a HALT_STB 216. HALT_STB 216 indicates whether differential data strobe transmit logic 114 is to operate in a normal operating mode (normal toggling of different data strobe signals 210, 212) or in a halt data strobe mode of operation (differential data strobe signals 210, 212 held in logical state). In addition, a STOP_STB_TRIGGER signal 214 indicates the precise time the differential data strobe 122 is to be halted. The state in which the data strobe 210 and the inverse data strobe 212 are halted is determined by the state of another input signal, ~~STOP_STB_HIGH~~ STOP_DS_HIGH 220.

A7

Paragaph at page 14, lines 3-11

Strobe stopping logic 202 includes primarily two functional elements, differential data strobe control logic 208 and pulse stretch logic 206. Pulse stretch logic 206 generates a data strobe stop signal STOP_STB 230 that remains in the asserted logical state for the duration in which the differential data strobe 122 is to be halted. The STOP_STB 230 signal is used by differential data strobe 122 is to transmit normally; that is, as ~~1 or 2 a pulsed~~ 1- or 2- pulse signals. It should be understood that there are a myriad of other techniques that one can implement to communicate such information.

A8

Paragraph at page 15, line 16 to page 16, line 1

In accordance with aspects of the present invention, the differential data strobe 122 is halted by virtue of control logic 208 changing the logical state of one or more of the logic level signals ~~222-228~~ 222, 224, 226, 228 provided to level select logic 204. As will described in detail below, when the differential data strobe 122 is to be halted with DS_OUT 210 asserted, then the logical state of GND_DS 224 is changed from a de-asserted state to an asserted state so that when signal generator 204 switches from VDD_DS 222 to GND_DS 224 to drive DS_OUT 210, the same asserted logical state is provided continually to signal generator 204. As a result, DS_OUT 210 is continually in the asserted state. Similarly, should the differential data strobe 12 be halted with DS_OUT 210 in the de-asserted state, then data strobe

A9 cont

control logic 208 changes the logical state of VDD_DS 222 from its asserted state to a de-asserted state so that when signal generator 204 switches from VDD_DS 222 to GND_DS 224, the same low logical state is provided to signal generator 204. This results in DS_OUT 210 having a continuous de-asserted logical state as it toggles between VDD_DS 222 and GND_DS 224. This same approach is implemented to control the inverse data strobe signal DSN_OUT 212 by adjusting the logical states of VDD_DSN 228 and GND_DSN 226.

A9 Cont

Paragraph at page 16, lines 21 to 26

To further insure such similar experiences the data transmitted over source synchronous link ~~116~~ 106 is "double pumped." That is, data is transmitted over the data link at twice the frequency as the differential data strobe 122. In the illustrative embodiment, the differential data strobe has a frequency of 250MHz. Thus, in this embodiment, DATA_OUT 234 operates at 500 MHz. A timing diagram illustrating the relationship between these signals is provided in Figure 2B.

A10

Paragaph at page 19, lines 6-13

The differential data strobe signals 210, 212 remain in their halted states until HALT_STB 216 transitions to a de-asserted state indicating that differential data strobe transmit logic 114 is to cease operating in the halt data strobe mode of operation and return to the normal ~~modes~~ mode of operation. HALT_STB 216 transitions to a logical low state during time period T5 that is latched at the next rising clock edge, time period T6. After a one cycle delay (time period T6), the differential data strobe signals DS_OUT 210 and DSN_OUT 212 return to normal operations at the next falling edge during time period T7.

A11

Paragaph at page 19, lines 19-23

As noted, pulse stretch logic 206 generates the data strobe stop signal STOP_STB 230 that is used by control logic 208 as described herein. Pulse stretch logic 206 receives as inputs the strobe halt mode signal HALT_STB 216 and the halting trigger STOP_STB_TRIGGER 214. Also, active low reset signal RESET_LOW ~~216~~ 218 is also provided to pulse stretch logic 206.

A12

Paragaph at page 20, lines 12-21

When the differential data strobe 122 is to be halted, HALT_STB 216 is asserted. Inverter 416 inverts HALT_STB 216. The inverted signal is referred to as HALT_STB_NOT 410. Thus, HALT_STB_NOT 410 is de-asserted during the halt data strobe mode of operation and is asserted during the normal operational mode. Similarly, RESET_LOW 218 is an active low signal and, therefore, is asserted in non-reset conditions. Inverter 418 inverts RESET_LOVE 218. The inverted signal is referred to as RESET_LOW_NOT 412. RESET_LOW_NOT 412 remains de-asserted during this example. As such, the output of NOR gate ~~408~~ 404, STOP_STB 230, will have the same logical state as the third input, INT_NODE_A ~~408~~ 408, until the device is reset or the data strobes are no longer halted.

A13

Paragraph at page 22, line 25 to page 22, line 8

In this embodiment of the present invention, the differential data strobe 122 is halted by virtue of control logic 208 changing the logical state of one or more of the logic level signals ~~222-228~~ 222, 224, 226, 228 provided to signal generator 204. As noted, when the differential data strobe 122 is to be halted with DS_OUT 210 asserted, then the logical state of GND_DS 224 is changed from a de-asserted state to an asserted state. When signal generator 204 switches from VDD_DS 222 to GND_DS 224 to transmit as DS_OUT 210, it thereafter receives the same asserted logical state. As a result, DS_OUT 210 is continually in that same asserted state. Similarly, should the differential data strobe 122 be halted with DS_OUT 210 in the de-asserted state, then data strobe control logic 208 changes the logical state of VDD_DS 222 from its asserted state to a de-asserted state. When signal generator 204 switches from VDD_DS 222 to GND_DS 224, the same low logical level is thereafter received, resulting in DS_OUT signal 210 having a continuous de-asserted logical state as it toggles between VDD_DS 222 and GND_DS 224. This same approach is implemented to control the inverse data strobe signal DSN_OUT 212 by adjusting the logical states of VDD_DSN 228 and GND_DSN 226.

A14

Paragraph at page 22 , lines 9 to 18

Turning now to the logic elements illustrated in Figure 6, control logic 208 includes four gates each generating one of the four logic level signals ~~22 228~~ 222, 224, 226, 228 as its output. Specifically, VDD_DS 222 is the output of a NAND gate 602 having the strobe stop signal STOP_STB 230 and the inverse of the data strobe halt high signal STOP_DS_HIGH_NOT ~~613~~ 614 provided as its inputs. GND_DS 224 is the output of a NOR gate 604 having the inverse of the stop strobe signal, STOP_STB_NOT 616, and STOP_DS_HIGH_NOT ~~613~~ 614 provided as its inputs. GND_DSN 226 is the output of a NOR gate 606 having STOP_STB_NOT 616 and STOP_DS_HIGH 220 provided as its inputs. VDD_DSN 228 is the output of a NAND gate 608 having STOP_STB 230 and STOP_DS_HIGH 220 as provided at its input ports.

A15

Paragraph at page 25, lines 2-7

In the example sequence illustrated in Figure 7, STOP_DS_HIGH signal 220 is asserted at time period T1. This indicates that when the differential data strobe is halted, that the data strobe signal DS_OUT 210 should be halted in the high logical state while the data strobe not signal DSN_OUT 212 should be halted in the low logical state. During time period T1, VDD_DS 222 is asserted, GND_DS 224 is de-asserted, VDD_DSN 228 is de-asserted and GND_DSN_226 ~~GND_DS_228~~ is asserted (that is, in normal mode).

A16

Paragraph at page 25, lines 8 to 18

Upon receipt of the stop strobe signal STOP_STB 230, certain of the level signals ~~222 228~~ 222, 224, 226, 288 are altered to accommodate the specified logic level for DS_OUT 210 and DSN_OUT 212. Since STOP_STB_HIGH 220 is asserted in this example, GND_DS 224 transitions from a de-asserted to an asserted state in time period T2. This is illustrated by arrows 702 and 704 in Figure 7. GND_DS 224 remains in this state until STOP-STB 230 is de-asserted. Thus, for time periods T2-T4, VDD_DS 222 and GND_DS 224 have the same asserted state. Thus, as level select logic 208 alternates between VDD_DS 222 and GND_DS 224 to drive DS_OUT 210, the same logic level is provided to control logic 208 during time periods T2-T4. When the differential data strobe is to no longer be halted,

A17 cont

A17 cont

STOP_STB 230 is de-asserted, causing GND_DS 224 to return to its normal de-asserted state. This is illustrated by arrow 706 in Figure 7.

Paragraph at page 28, lines 16 to 25

A18

In this exemplary sequence of waveforms, from time period T2 through time period T4 transmitter 108 is in the halt data strobe mode of operation. The specified logic levels of signals ~~22-228~~ 222, 224, 226, 288 is such that DS_OUT 210 will be halted in the asserted state while DSN_OUT 212 will be halted in the de-asserted state. To achieve this, GND_DS 224 transitions from a de-asserted to an asserted state for these time periods as shown in Figure 9. As a result, both, VDD_DS 222 and GND_DS 224 to transmit as DS_SELECT 842. With both such signals in the asserted state the selection of either will cause DS_SELECT 832 to be continually in the asserted state; that is, halted in the asserted state.

Paragraph at page 29, lines 3 to 30

A19

The corresponding latched signals 828, 830, 836, 838 and 840 are also illustrated in Figure 900. As shown, the signal level signals ~~222-228~~ 222, 224, 226, 228 are passed through their respective transparent latch when CLK250 116 is de-asserted due to the use of the inverse clock signal CLK250_NOT 826 to provide the clock input to latches 802-808. Since GND-DS 224 and VDD_DSN 228 transition at a rising edge of CLK250 116, there is a half cycle delay between the latched signals 828, 830, 836 and 838 and the signals ~~222-228~~ 222, 224, 226, 228. One example of this is illustrated by arrow 912 sho3ing the relationship between the rising edge of GND_DS 224 and the subsequent rising edge of GND_DS_250_LA 830.

Paragraph at page 33, lines 4 to 8

A20

DATA_OUT 234 is received by a receiver 1012 and passed through a multiplexer ~~100~~ 1006. Multiplexer 1006 selects either DATA_OUT 234 or an unrelated signal based on criteria not-relevant to the present invention. Similarly, DS_OUT 210 and DSN_OUT 212 are received by receivers 1014 and 1016 and passed through multiplexers 1008 and 1010. Multiplexers 1008 ad 1010 are controlled similarly.

Paragraph at page 33, lines 9 to 14

A21

DS_OUT 210 is used to latch data capture flip-flop 1002A while DSN_OUT 212 is used to latch data capture flip-flop 212. Thus 2 bits of data are latched with each data strobe clock cycle. The rising edge of the differential data are latched with each data strobe clock cycle. The rising edge of the differential data strobe DS_OUT 210 clocks flip-flop ~~1002~~ 1002A while the rising edge of DSN_OUT 212 clocks flip-flop 1002B. With this approach, the data capture flip-flops latch in 2 bits of data in a single data strobe cycle; that is 2 bits per 250 MHz, or 500 MHz.

Paragraph at page 33, line 25 to page 34, line 3

A22

In accordance with one aspect of the invention, DATA-OUT 234 and differential data strobe signals DS_OUT 210 and DSN_OUT 212 are processed through the same logical and physical components in source synchronous receiver 110. Thus, driver 1012 is identical to driver 1014 and 1016. Similarly, multiplexer 1006 is identical to multiplexer 1008 and ~~110~~ 1010, and the select line is driven by the same local clock. For the reason set forth above, in certain implementations of source synchronous receiver 110, a delay and fanout tree 1004 is implemented to compensate for delays across such receivers. As noted, this insures injected link noise is experienced by both, DATA_OUT signal 234 and the differential data strobe signals 122.

Paragraph at page 34, lines 20-27

A23

Further features of the present invention are described in commonly-owed U. S. Utility Patent Application No. 09/560,364 entitled "A SOURCE SYNCHRONOUS LINK WTH DATA AND CLOCK SIGNAL SHAVING THE SAME ELECTRICAL CHARACTERISTICS" naming as inventors Karen Lo, Jeffery A. Benis and Allan R. Desroches, filed concurrently herewith ~~under Attorney Docket No. 10002534.1,~~ the specification of which is herein incorporated by reference.